

ENGPYHS 2E04: Lab XIntroduction

In this lab, I used sequential logic design to design a circuit that displays my student number on loop. In the analytical portion, I converted the decimal numbers to Boolean form and generated a state transition table to determine the inputs for the JK flipflops. I then created K-maps based off the state transition table to design Boolean logic expressions for the inputs. I proceeded to use Multisim to build the circuit using the logic expressions and used the seven segment display to verify that the logic produces the student number. Finally in the physical section, I built the circuit and used the seven segment display again to verify the logic.

Analytical

I converted the decimal numbers in my student number to Boolean form and used the excitation table to produce a state transition table. My student number is: 400307169.

Table 1: Student Number

Number	4	0	0	3	0	7	1	6	9
Boolean Number	0100	0000	0000	0011	0000	0111	0001	0110	1001

Table 2: JK Excitation Table

q (current state)	Q (next state)	J	$\bar{K}$
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

I require four flipflops to produce 4-bit numbers. I can't eliminate any flipflops since none of the bits are high, low or equal to a combination of other bits. I also need two counter flipflops for the zeroes that repeat three times to identify which zero is occurring in the sequence. I proceeded to generate a state transition table using Tables 1 and 2. I randomly chose the counter numbers and ensured to avoid the use of "don't care" counters to simplify the possibilities of the flipflop inputs.

Table 3: State Transition Table

$q_1$	$q_2$	$q_3$	$q_4$	$q_5$	$q_6$	$Q_1$	$Q_2$	$Q_3$	$Q_4$	$Q_5$	$Q_6$	$J_1$	$\bar{K}_1$	$J_2$	$\bar{K}_2$	$J_3$	$\bar{K}_3$	$J_4$	$\bar{K}_4$	$J_5$	$\bar{K}_5$	$J_6$	$\bar{K}_6$
0	1	0	0	1	0	0	0	0	0	1	0	0	X	X	0	0	X	0	X	X	1	0	X
0	0	0	0	1	0	0	0	0	0	0	1	0	X	0	X	0	X	0	X	X	0	1	X
0	0	0	0	0	1	0	0	1	1	1	0	0	X	0	X	1	X	1	X	1	X	X	0
0	0	1	1	1	0	0	0	0	0	1	1	0	X	0	X	X	0	X	0	X	1	1	X
0	0	0	0	1	1	0	1	1	1	1	0	0	X	1	X	1	X	1	X	X	1	X	0
0	1	1	1	1	0	0	0	0	1	0	1	0	X	X	0	X	0	X	1	X	0	1	X
0	0	0	1	0	1	0	1	1	0	1	0	0	X	1	X	1	X	X	0	1	X	X	0
0	1	1	0	1	0	1	0	0	1	0	0	1	X	X	0	X	0	1	X	X	0	0	X
1	0	0	1	0	0	0	1	0	0	1	0	X	0	1	X	0	X	X	0	1	X	0	X

The following inputs are either high, low or another output. These conclusions were made using inspection.

$$\bar{K}_1 = 0$$

$$\bar{K}_2 = 0$$

$$J_3 = q_6$$

$$\overline{K_3} = 0$$

$$\overline{K_4} = q_2$$

$$J_5 = 1$$

$$\overline{K_6} = 0$$

The next step was to produce a K-map for the flipflop inputs that do not have an input of high, low or another output. I used the sum of products method to derive the Boolean logic expressions. I've color coded the state transition table again to correspond with boxes on the K-maps.

$q_1$	$q_2$	$q_3$	$q_4$	$q_5$	$q_6$	$Q_1$	$Q_2$	$Q_3$	$Q_4$	$Q_5$	$Q_6$	$J_1$	$\overline{K_1}$	$J_2$	$\overline{K_2}$	$J_3$	$\overline{K_3}$	$J_4$	$\overline{K_4}$	$J_5$	$\overline{K_5}$	$J_6$	$\overline{K_6}$
0	1	0	0	1	0	0	0	0	0	1	0	0	X	X	0	0	X	0	X	X	1	0	X
0	0	0	0	1	0	0	0	0	0	0	1	0	X	0	X	0	X	0	X	X	0	1	X
0	0	0	0	0	1	0	0	1	1	1	0	0	X	0	X	1	X	1	X	1	X	X	0
0	0	1	1	1	0	0	0	0	0	1	1	0	X	0	X	X	0	X	0	X	1	1	X
0	0	0	0	1	1	0	1	1	1	1	0	0	X	1	X	1	X	1	X	X	1	X	0
0	1	1	1	1	0	0	0	0	1	0	1	0	X	X	0	X	0	X	1	X	0	1	X
0	0	0	1	0	1	0	1	1	0	1	0	0	X	1	X	1	X	X	0	1	X	X	0
0	1	1	0	1	0	1	0	0	1	0	0	1	X	X	0	X	0	1	X	X	0	0	X
1	0	0	1	0	0	0	1	0	0	1	0	X	0	1	X	0	X	X	0	1	X	0	X

Table 4:  $J_1$  K-map

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1 q_2 \backslash q_3 q_4$	00	01	11	10		00	01	11	10
0	00	X	X	X	X	00	0	0	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	0	X	0	X	00	0	X	X	X
1	01	0	X	0	1	01	X	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_1 = q_5 \overline{q_6} q_3 \overline{q_4}$$

Table 5:  $J_2$  K-map

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1 q_2 \backslash q_3 q_4$	00	01	11	10		00	01	11	10
0	00	X	X	X	X	00	0	1	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	1	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	0	X	0	X	00	1	X	X	X
1	01	X	X	X	X	01	X	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_2 = \overline{q_5} \overline{q_6} q_4 + \overline{q_5} \overline{q_6} + q_5 q_6 = \overline{q_5} (q_4 + \overline{q_6}) + q_5 q_6$$

Table 6:  $J_4$  K-map

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2 \backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	X	X	X	X	00	1	X	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	0	X	X	X	00	1	X	X	X
1	01	0	X	X	1	01	X	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_4 = q_5 \bar{q}_6 q_3 + q_6 = q_5 q_3 + q_6$$

Table 7:  $\bar{K}_5$  K-map

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2 \backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	X	X	X	X	00	X	X	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	0	X	1	X	00	1	X	X	X
1	01	1	X	0	0	01	X	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$\bar{K}_5 = q_5 \bar{q}_6 \bar{q}_3 q_2 + q_5 \bar{q}_6 q_3 \bar{q}_2 + q_5 q_6$$

Table 8:  $J_6$  K-map

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2 \backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	X	X	X	X	00	X	X	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	0	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	1	X	1	X	00	X	X	X	X
1	01	0	X	1	0	01	X	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_6 = \bar{q}_2 q_5 \bar{q}_6 + q_5 \bar{q}_6 q_4$$

I noticed that all the Boolean logic expressions derived from the K-maps are very complicated and decided to choose new counter values to obtain simpler expressions.

Table 9: State Transition Table

$q_1$	$q_2$	$q_3$	$q_4$	$q_5$	$q_6$	$Q_1$	$Q_2$	$Q_3$	$Q_4$	$Q_5$	$Q_6$	$J_1$	$\overline{K_1}$	$J_2$	$\overline{K_2}$	$J_3$	$\overline{K_3}$	$J_4$	$\overline{K_4}$	$J_5$	$\overline{K_5}$	$J_6$	$\overline{K_6}$
0	1	0	0	1	1	0	0	0	0	0	0	0	X	X	0	0	X	0	X	X	0	X	0
0	0	0	0	0	0	0	0	0	0	1	1	0	X	0	X	0	X	0	X	1	X	1	X
0	0	0	0	1	1	0	0	1	1	1	0	0	X	0	X	1	X	1	X	X	1	X	0
0	0	1	1	1	0	0	0	0	0	0	1	0	X	0	X	X	0	X	0	X	0	1	X
0	0	0	0	0	1	0	1	1	1	1	0	0	X	1	X	1	X	1	X	1	X	X	0
0	1	1	1	1	0	0	0	0	1	0	1	0	X	X	0	X	0	X	1	X	0	1	X
0	0	0	1	0	1	0	1	1	0	1	0	0	X	1	X	1	X	X	0	1	X	X	0
0	1	1	0	1	0	1	0	0	1	0	1	1	X	X	0	X	0	1	X	X	0	1	X
1	0	0	1	0	1	0	1	0	0	1	1	X	0	1	X	0	X	X	0	1	X	X	1

The following inputs are either high, low or another output. These conclusions were made using inspection.

$$\overline{K_1} = 0$$

$$\overline{K_2} = 0$$

$$\overline{K_3} = 0$$

$$\overline{K_4} = q_2$$

$$J_5 = 1$$

$$J_6 = 1$$

$$\overline{K_6} = q_1$$

Here are the K-maps for the remaining inputs and their Boolean logic expressions using Sum of Products. I used the color coded state transition table again to match boxes with the K-maps.

Table 10:  $J_1$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1 q_2 \backslash q_3 q_4$	00	01	11	10		00	01	11	10
0	00	0	X	X	X	00	0	0	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	0	X	00	0	X	X	X
1	01	X	X	0	1	01	0	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_1 = q_5 \overline{q_6} \overline{q_4}$$

Table 11:  $J_2$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2$	00	01	11	10		00	01	11	10
	$\backslash q_3q_4$									
0	00	0	X	X	X	00	1	1	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	1	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	0	X	00	0	X	X	X
1	01	X	X	X	X	01	X	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_2 = \overline{q_5}q_6$$

Table 12:  $J_3$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2$	00	01	11	10		00	01	11	10
	$\backslash q_3q_4$									
0	00	0	X	X	X	00	1	1	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	0	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	X	X	00	1	X	X	X
1	01	X	X	X	X	01	0	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_3 = \overline{q_5}q_6\overline{q_1} + q_5q_6\overline{q_2} = q_6(\overline{q_5}\overline{q_1} + q_5\overline{q_2})$$

Table 13:  $J_4$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2$	00	01	11	10		00	01	11	10
	$\backslash q_3q_4$									
0	00	0	X	X	X	00	1	X	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	X	X	00	1	X	X	X
1	01	X	X	X	1	01	0	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_4 = q_5\overline{q_6} + q_6(\overline{q_2} + \overline{q_5})$$

Table 14:  $\overline{K_5}$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2$ $\backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	X	X	X	X	00	X	X	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	0	X	00	1	X	X	X
1	01	X	X	0	0	01	0	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$\overline{K_5} = q_5 q_6 \overline{q_2}$$

I then used the K-maps to perform product of sums.

Table 15:  $J_1$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2$ $\backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	0	X	X	X	00	0	0	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	0	X	00	0	X	X	X
1	01	X	X	0	1	01	0	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_1 = \overline{q_5}(q_5 + \overline{q_6} + q_4)(q_5 + q_6)$$

Table 16:  $J_2$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2$ $\backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	0	X	X	X	00	1	1	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	1	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	0	X	00	0	X	X	X
1	01	X	X	X	X	01	X	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_2 = (\overline{q_5} + \overline{q_6})q_5$$

Table 17:  $J_3$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2 \backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	0	X	X	X	00	1	1	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	0	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	X	X	00	1	X	X	X
1	01	X	X	X	X	01	0	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_3 = (\overline{q_5} + \overline{q_6})(\overline{q_5} + q_6 + q_1)(q_5 + q_6 + q_2)$$

Table 18:  $J_4$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2 \backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	0	X	X	X	00	1	X	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	X	X	00	1	X	X	X
1	01	X	X	X	1	01	0	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$J_4 = (\overline{q_5} + \overline{q_6})(q_5 + q_6 + q_2)$$

Table 19:  $\overline{K_5}$  Input

	$q_6$	0	0	0	0		1	1	1	1
$q_5$	$q_1q_2 \backslash q_3q_4$	00	01	11	10		00	01	11	10
0	00	X	X	X	X	00	X	X	X	X
0	01	X	X	X	X	01	X	X	X	X
0	11	X	X	X	X	11	X	X	X	X
0	10	X	X	X	X	10	X	X	X	X
		00	01	11	10		00	01	11	10
1	00	X	X	0	X	00	1	X	X	X
1	01	X	X	0	0	01	0	X	X	X
1	11	X	X	X	X	11	X	X	X	X
1	10	X	X	X	X	10	X	X	X	X

$$\overline{K_5} = (q_5 + \overline{q_6})(q_5 + q_6 + q_2)$$

After looking at the POS and SOP Boolean logic expressions based off the second state transition diagram, I chose to use the POS expressions because they are simpler. Here are the final flipflop inputs:

sundarek

Kavya Sundaresan

400307169

$$J_1 = q_5 \overline{q_6} \overline{q_4}$$

$$\overline{K_1} = 0$$

$$J_2 = \overline{q_5} q_6$$

$$\overline{K_2} = 0$$

$$J_3 = q_6 (\overline{q_5} \overline{q_1} + q_5 \overline{q_2})$$

$$\overline{K_3} = 0$$

$$J_4 = q_5 \overline{q_6} + q_6 (\overline{q_2} + \overline{q_5})$$

$$\overline{K_4} = q_2$$

$$J_5 = 1$$

$$\overline{K_5} = q_5 q_6 \overline{q_2}$$

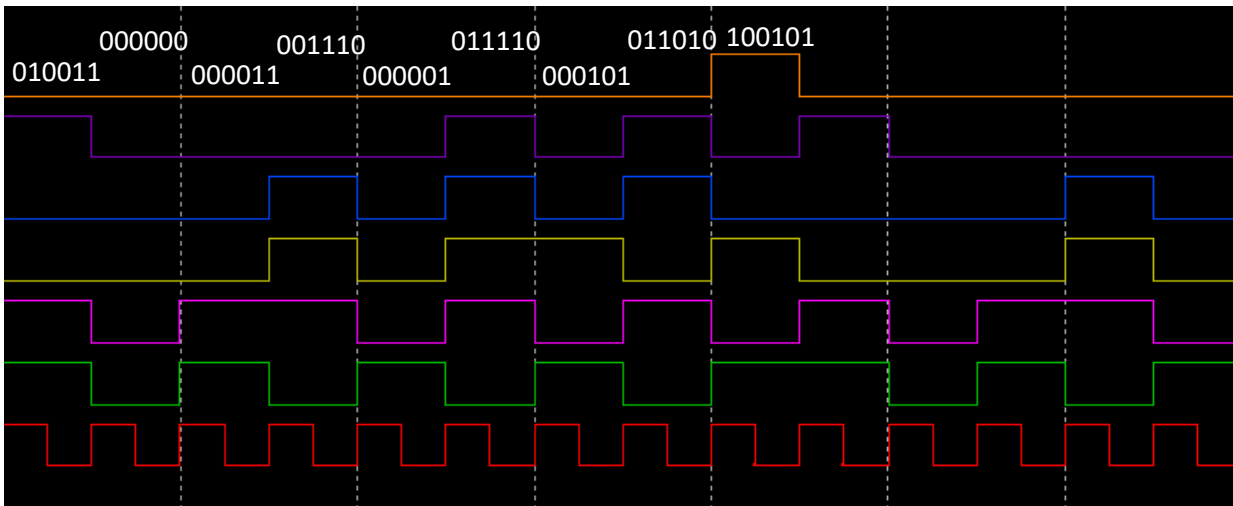
$$J_6 = 1$$

$$\overline{K_6} = q_1$$



Intermediate connections between gates are in grey. For inputs that are not directly connected straight to another output pin/VCC/Ground, J inputs are cyan and  $\bar{K}$  inputs are light brown. The decoder chip takes the output of flipflops 1-4 and connects it to the seven segment display through 1 k $\Omega$  resistors.

I used the logic analyzer to generate a timing diagram of the states.

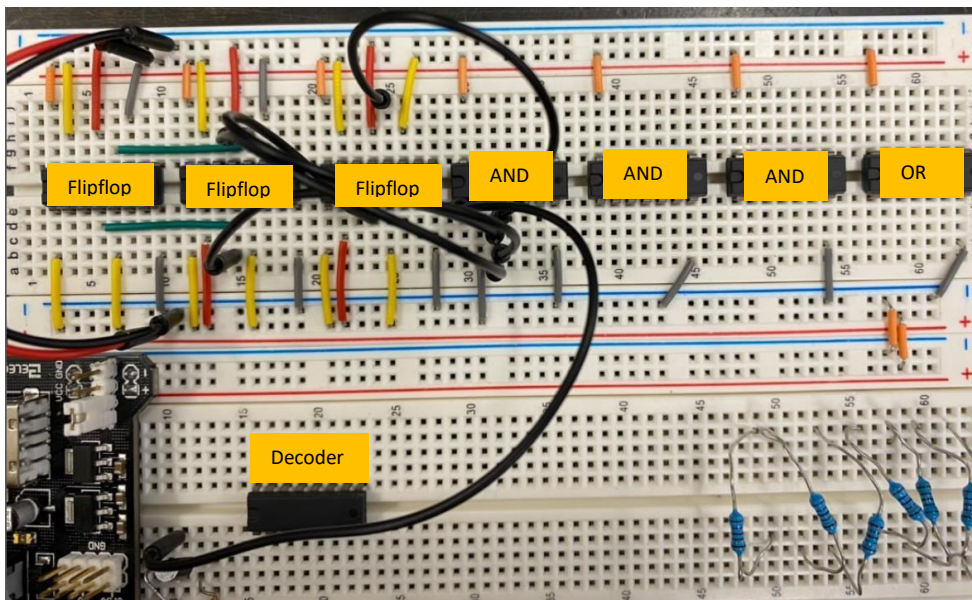


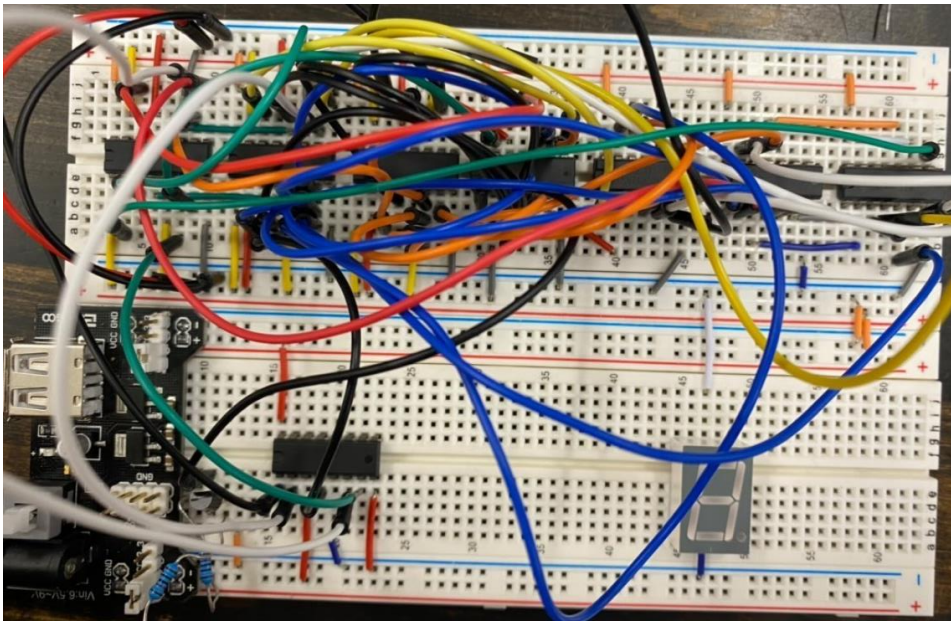
The Multisim timing diagram matches the state transition table from the analytical and the display correctly shows my student number.

**Multisim Demo:** [https://youtu.be/d57b\\_jCpWmc?t=96](https://youtu.be/d57b_jCpWmc?t=96)

### Physical

I built my circuit using two breadboards, 3 flipflop chips, 3 AND chips, 1 OR chip, 1 decoder chip and a seven segment display. Here is the setup for my first attempt at building the circuit:





The above build didn't function properly so I began troubleshooting. First, I checked the clock signal and the voltage in the header boards which were both as expected.

Clock Signal



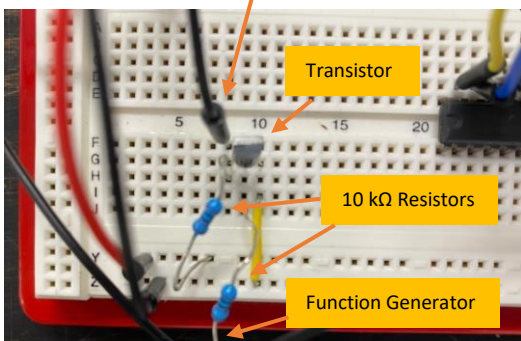
Header Board Voltage



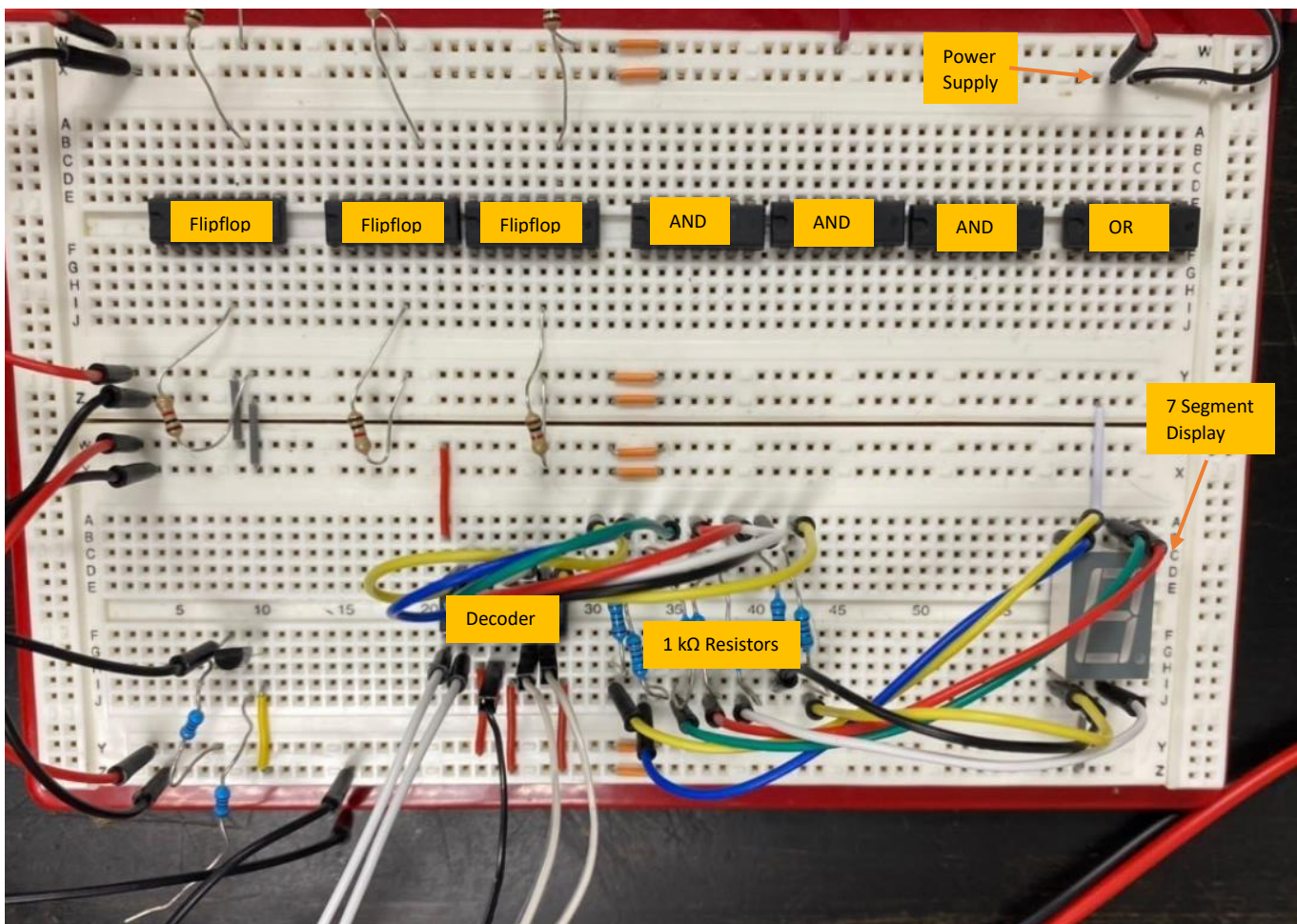
I then had Peter test all my chips using his equipment and they were all in good condition. My next step was to check if the display was working properly. So I disconnected the flipflop outputs from the decoder chip and set the clock pin to high. I manually forced in numbers 0-10 to check if the display properly showed the numbers and at that point I noticed that a couple of the segments were never turning on. Peter and I used the Hantek to measure the voltage at the pins on the decoder chip and on the display that match up with the segment on the display that wasn't working. We noticed that the voltage at these pins were zero, however the voltage on the decoder chip's leg at that pin was high. So the voltage from the decoder chip was not transferring to the breadboard. I went on to test a few other areas of the breadboard and noticed that for some reason components weren't making proper contact with certain rows of the board. Thus, Peter let me borrow one of the expensive breadboards and I rebuilt the circuit. Here is the setup process of the working circuit.

Here is the clock signal built using a transistor and two 10 k $\Omega$  resistors.



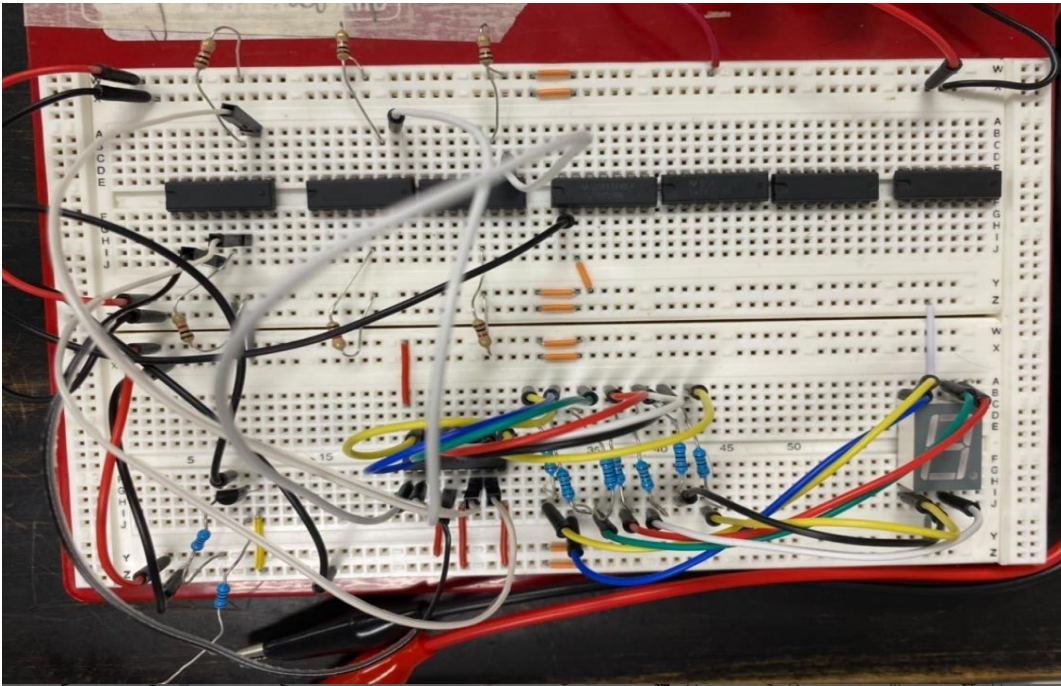


Here is the placement of the chips. In this step, I've also wired up the decoder chip to the seven segment display and I've allotted white wires to be connected to the flipflop outputs. I've connected the not preset pins on all the flipflops to high through a 1 kΩ resistor so I can easily force an output later on if needed by touching the resistors with a jumper whose other end is connected to ground to force that flipflop to output a one. Notice that I've used solid wires and jumper wires to connect power and ground between the appropriate rails. Black wires here represent ground while red wires represent VCC. I used an external power supply to power my circuit and used the Hantek's probes to be certain that all the header rails had the appropriate voltages.

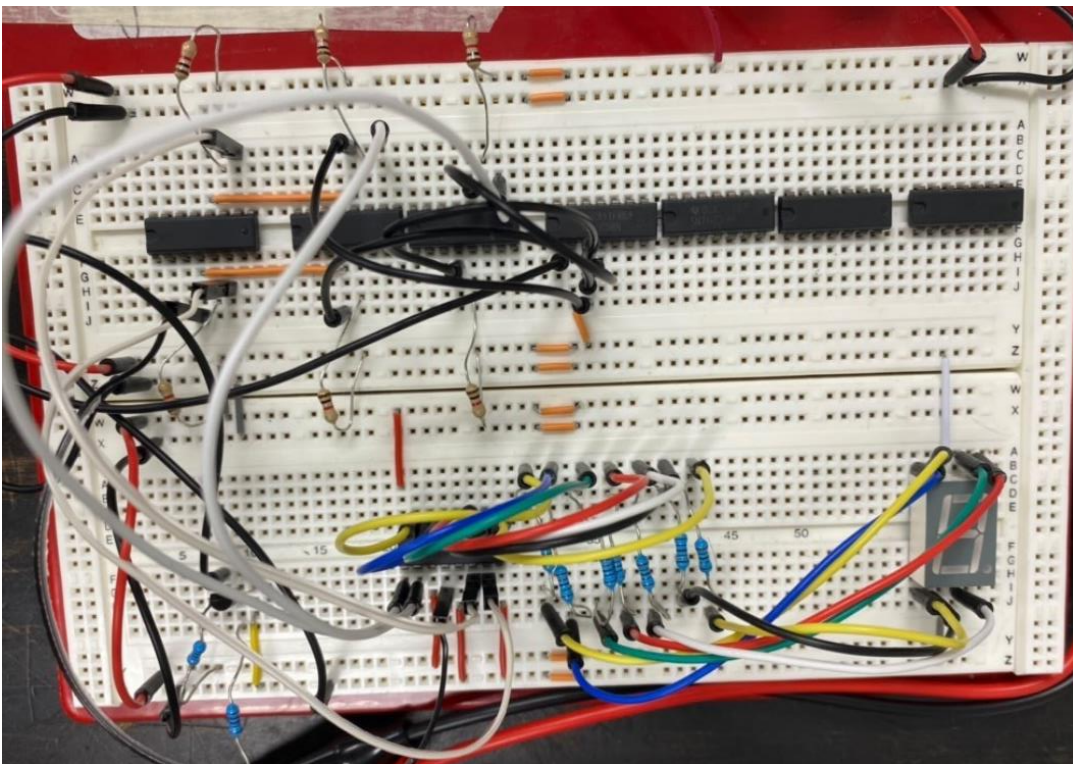


Next I connected the white wires on the decoder chip to the appropriate flipflop outputs. I've taken the clock output from the transistor and put it through an AND gate where the other input is high.



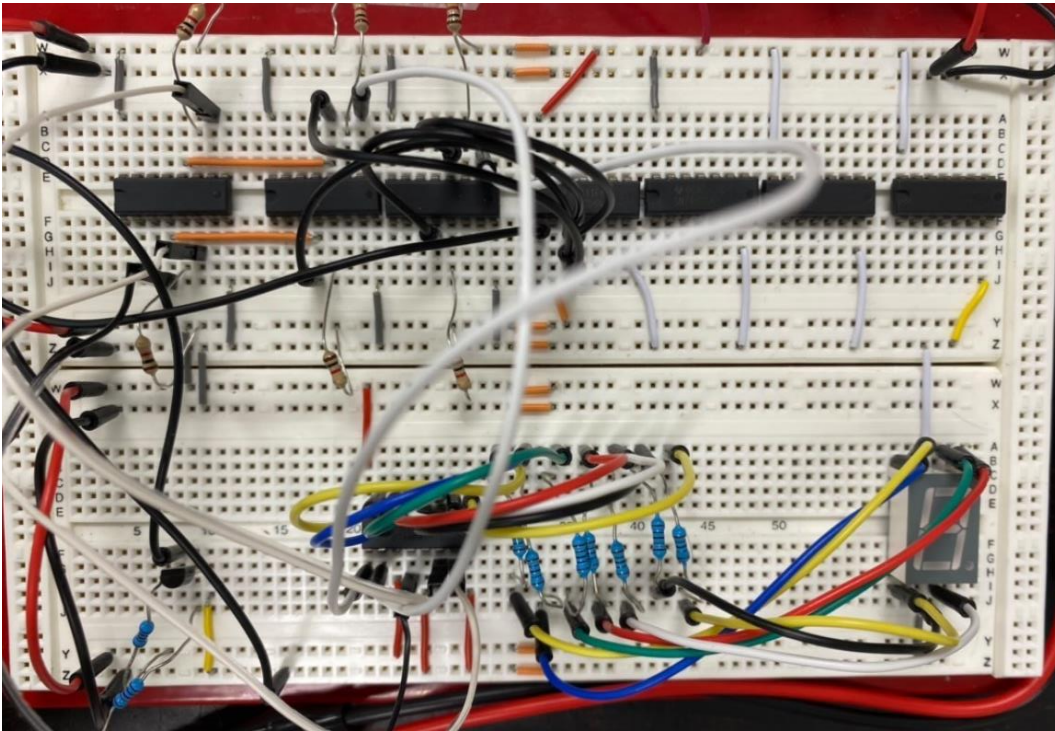


The output of the AND gate was put into all the clock pins on the flipflops as well as the clock pin on the decoder chip. Notice that the majority of the clock wiring is done in black. I did however use solid orange wires for the clock pins on the left most flipflop. Through out my build I attempted to use as many solid wires as possible to avoid clutter. I measured the clock pulse again from the output of the AND gate and it was functioning properly.

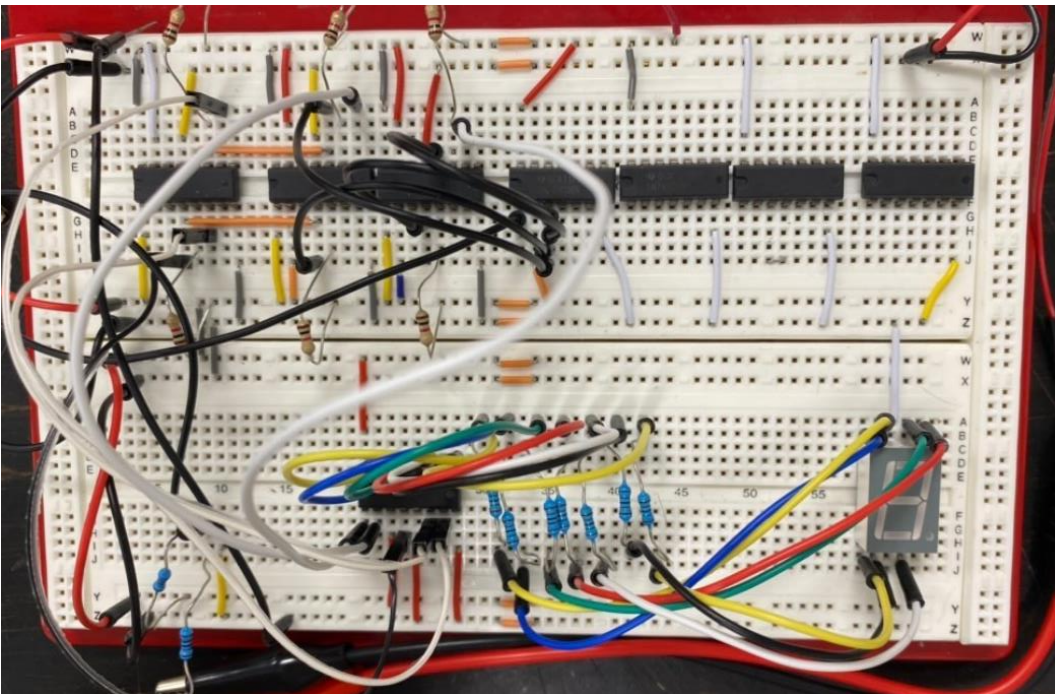


Here I've used solid wires to hook up all the VCC and not clear pins to high as well as all the ground pins to low on the top breadboard.





From here on I began to wire up the flipflops and gates using my logic derived in the analytical portion. First I connected all inputs that were high or low using solid wires.



Here is the color scheme that was used to wire up all remaining inputs:

- Green - J inputs
- Yellow -  $\bar{K}$  inputs
- White -  $J_1$  logic
- Purple -  $J_2$  logic

Orange -  $J_3$  logic

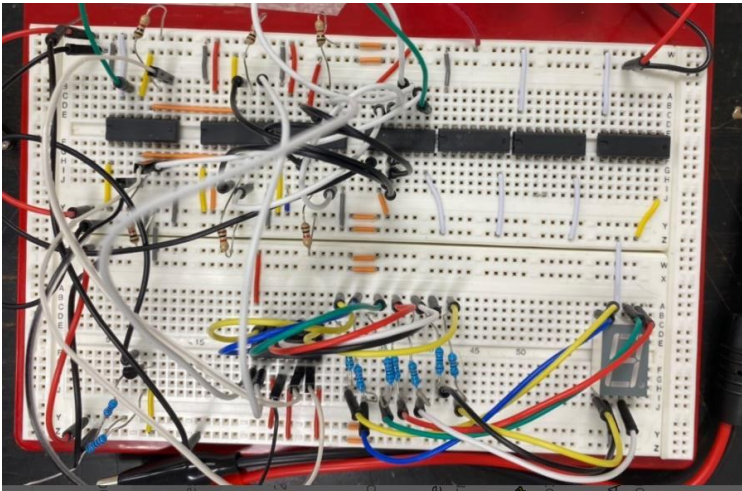
Blue -  $J_4$  logic

Brown -  $\overline{K_4}$  and  $\overline{K_6}$

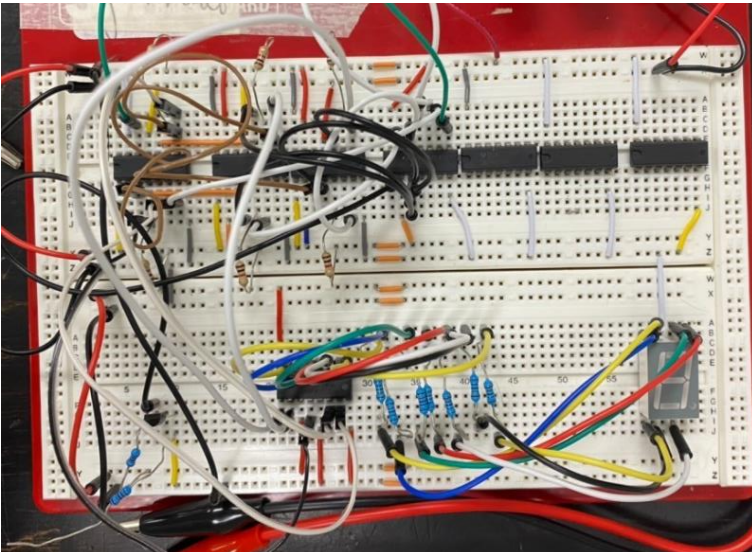
Red -  $\overline{K_5}$

Note that solid wires were used when possible instead of following the above color code to reduce clutter and their colors are noted in the wiring diagram. Furthermore, the input to  $J_3$  is orange because I didn't have enough long green wires. I chose the above color scheme because it made it easier for me to verify the wiring for each input since all the wires making up the input would be of the same color.

$J_1$  wiring:

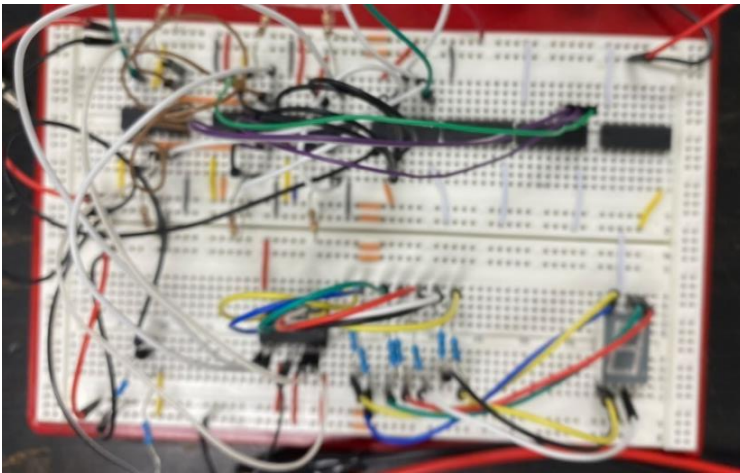


$\overline{K_4}$  and  $\overline{K_6}$  wiring:

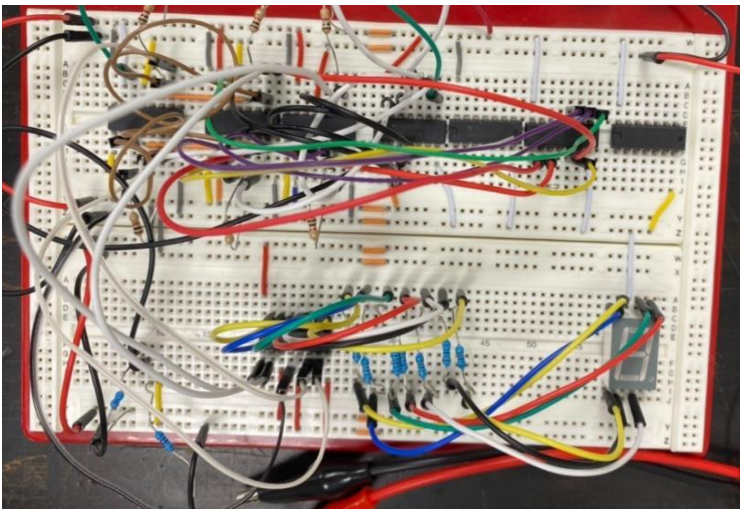


$J_2$  wiring:

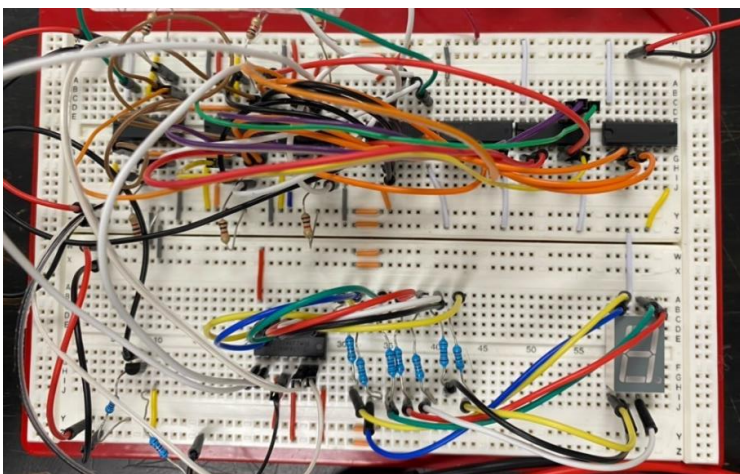




$\overline{K_5}$  wiring:

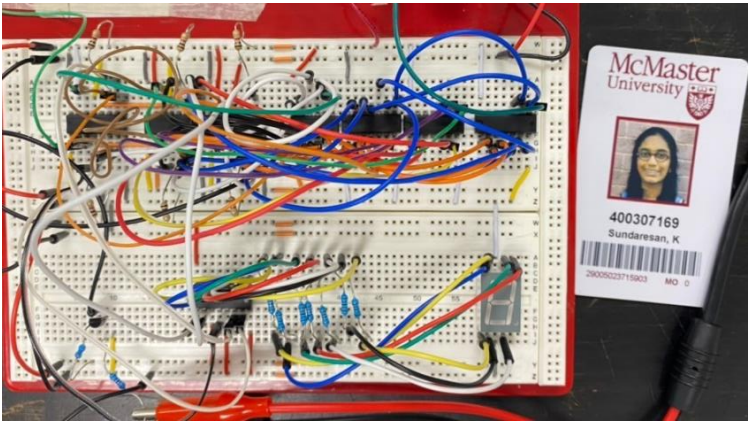


$J_3$  wiring:

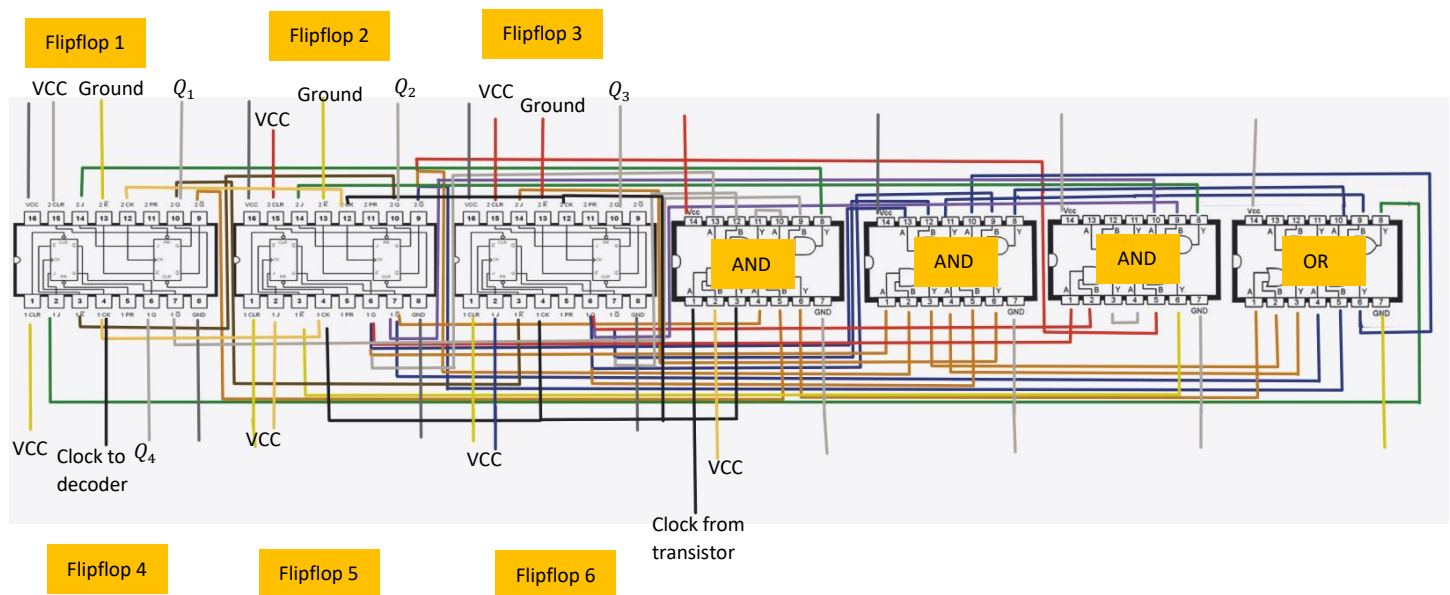


Final Circuit and  $J_4$  wiring:





Wiring diagram:



Note that light grey represents white wires on the board and dark grey represents grey solid wires. All of the VCC pins on the chips were connected to high and all the ground pins were connected to low

My final circuit worked out to display my student number on loop correctly.

**Physical Demo:** [https://youtu.be/d57b\\_jCpWmc?t=159](https://youtu.be/d57b_jCpWmc?t=159)

**Presentation:** [https://youtu.be/d57b\\_jCpWmc](https://youtu.be/d57b_jCpWmc)